CLAIMS:

1. (amended) A timing adjusting method ~~characterized by the fact that in~~ comprising a timing adjusting method for adjusting the timing of an event, said timing adjustment of said event is performed based on multiphase clocks.

2. (amended) The timing adjustment method described in Claim 1 ~~characterized by the fact that~~ wherein said event is an electrical event, which refers to at least one transition that takes place between plural electrical states.

3.- 9. (canceled)

10. (amended) A timing adjustment method ~~characterized by the following facts:~~ comprising:

~~in a timing adjustment method for adjusting the timing of an event, there are the following steps:~~

[[a]] generating multiphase clock signals ~~generating step for generating multiphase clocks~~, with said multiphase clock[[s]] signals comprising ~~composed of~~ plural phase clocks of different phases that represent plural different timing adjustment quantities applied on said event,

using said [[and a]] multiphase clock [[use step]] signals in which any one said phase clock signal from said multiphase clock[[s]] signals is used, and an event change timing signal representing the changed timing of said event is generated.

11.- 12 (canceled)

13. (amended) The timing adjustment method described in Claim 10 ~~or 11~~ wherein ~~characterized by the fact that it also has the fact that~~ said multiphase clock ~~generating~~ generation ~~step also contains~~ comprises generating ~~a step in which~~ said multiphase clocks ~~are generated~~ in synchronization with a reference signal related to said events.

14. (amended) The timing adjustment method described in Claim ~~13 characterized by the fact that~~ 4 wherein said multiphase clock is composed of plural phase clocks with equal spacing between them.

15. (canceled)

16. (amended) The timing adjustment method described in Claim [[14]] 1 wherein said events are events on an optical disk recording medium~~.~~which are rise events and fall events of the write pulses in the pulse width adjustment of the write pulses for writing on said optical disk recording medium; said write pulses are for determining the timing of control of output of the laser used in write on said optical disk recording medium.

17. - 18. (canceled)

19. (amended) The timing adjustment method described in Claim 16 further comprising generating ~~17 characterized by the fact that there is also a step in which~~ write pulses after a timing change are generated from said event change timing signal and wherein said multiphase clock generation comprises said reference signal being related to said events is obtained from the wobble signal of said optical disk recording medium..

20. (canceled)

21. (amended) The timing adjustment method described in Claim 1 wherein ~~any of Claims 14-20 characterized by the fact that~~ said optical disk recording medium has a rotation control system, such as a CAV system, zone CLV system, or CLV system.

22. (canceled)

23. (amended) The timing adjustment method described in Claim 1 wherein ~~22 characterized by the fact that~~ said multiphase clocks are generated from the transmission

clock of said digital transmission data[[.]], and wherein an adjustment quantity input that assigns the timing adjustment quantity applied on said events is received, and selecting one said phase clock having said timing adjustment quantity corresponding to said adjustment quantity input is selected as said event change timing signal.

24.-27 (canceled)

28. (amended) A timing adjustment circuit ~~characterized by the fact that a timing adjustment circuit~~ for adjusting the timing of events is ~~composed of the following means~~ comprising:

a multiphase clock generator ~~generating means~~ for generating multiphase clocks, with said multiphase clocks composed of plural phase clocks having different phases representing plural different adjustment quantities applied on said events,

and a multiphase clock use [[means]] circuit that uses any one said phase clock selected from said multiphase clocks and generates an event change timing signal representing the changed timing of said events.

29. (amended) [[A]] The timing adjustment circuit ~~for an event group characterized by the fact that~~ of Claim 28 wherein the timing adjustment circuit for an event group adjusts the timing of one event group composed of plural events has, ~~and it consists of the following means:~~ an event decomposition [[means]] circuit that decomposes said event group into individual events[[,]] ; and a synthesis circuit that receives said event change timing signals generated by said timing adjustment circuits for said events in said event group and synthesizes them to generate a synthetic event change timing signal.

~~and an event group timing adjustment means composed of timing adjustment circuits described in Claim 28 for said various events, respectively.~~

30. (canceled)

31. (amended) The timing adjustment circuit described in Claim 28 wherein ~~30 characterized by the fact that~~ said timing adjustment circuits set for said events, respectively, contain a common multiphase clock generator.~~generating means.~~

32. (amended) The timing adjustment circuit described in Claim 28 further comprising ~~28 or 29 characterized by the fact that it also~~ a generator ~~contains a means~~ for generating an event timing signal that represents timing of said events, with said event timing signal in synchronization with said multiphase clocks.

33.-34. (canceled)

35. (original) The timing adjustment circuit described in Claim 28 wherein ~~34 characterized by the fact that~~ said multiphase clock use means contains an enlarging [[means]] circuit that receives said event timing signal and, by delaying the event timing signal, enlarges said timing adjustment quantity by [[means]] using of said multiphase clocks alone.

36. (amended) The timing adjustment circuit described in Claim 28 wherein ~~28 or 29 characterized by the fact that~~ said multiphase clock ~~generating means contains~~ generator comprises a PLL circuit [[means]] that generates said multiphase clocks in synchronization with the reference signal pertaining to said events.

37. (amended) The timing adjustment circuit described in Claim 36 wherein ~~36 characterized by the fact that~~ said events are events on an optical disk recording medium[[.]] , and wherein said events on the optical disk recording medium are rise events and fall events of the write pulses for write on said optical disk recording medium in pulse width adjustment of said write pulses, and said write pulses are for determining the timing for control of output of a laser used in write on said optical disk recording medium.

38. (canceled)

39. (amended) The timing adjustment circuit described in Claim 38 wherein ~~38 characterized by the fact that~~ said event timing signal ~~generating means~~ generator generates said event timing signal from said write pulses and wherein said multiphase clock use circuit also contains a generator for generating write pulses after a timing change from said event change timing signal.

40. (canceled)

41. (amended) The timing adjustment circuit described in Claim 36 wherein ~~any of Claims 36-40 characterized by the fact that~~ said multiphase clock ~~generating means~~ generator contains a circuit [[a means]] for obtaining a reference signal pertaining to said events from the wobble signal of said optical disk recording medium.

42. (amended) The timing adjustment circuit described in Claim 41 wherein ~~41 characterized by the fact that~~ said optical disk recording medium has a rotation control system, such as a CAV system, zone CLV system, or CLV system.

43. (amended) The timing adjustment circuit described in Claim 10 wherein ~~28 or 29 characterized by the fact that~~ said multiphase clock use [[means]] circuit contains ~~the following means:~~ [[a means]] a receiver for receiving an adjustment quantity input that assigns the timing adjustment quantity applied on said events, and a ~~selection means~~ selector that selects one said phase clock having said timing adjustment quantity corresponding to said adjustment quantity input as said event change timing signal from said multiphase clocks.

44.-46. (canceled)

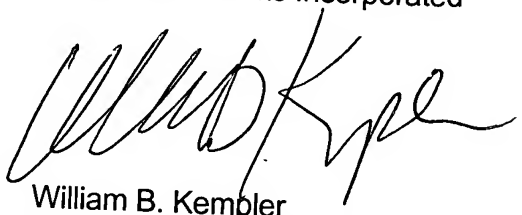
47. (amended) The timing adjustment circuit described in Claim 46 wherein the timing adjustment circuit is in an ~~The optical disk recorder described in Claim 46~~

~~characterized by the fact that said~~ optical disk recorder which is a CD-R, CD-RW, DVD-R, DVD-RW, DVD+R, DVD+RW or DVD-RAM device.

48. (canceled)

Respectfully submitted,

Texas Instruments Incorporated



William B. Kempler
Senior Corporate Patent Counsel
Reg. No.: 28,228
(972) 917-5452